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Claims

[c1] A method of forming a layer of interconnect in an integrated circuit comprising the steps of:
depositing a first layer of interlayer dielectric on a lower layer of said integrated circuit above a set of lower alignment marks;
depositing a first hardmask layer of TaN on said first layer of ILD, said first layer being substantially transparent in a relevant wavelength range;
forming an upper set of alignment marks;
patterning said ILD through said hardmask layer to form a set of apertures in said ILD; and
forming a conductive interconnect in said set of apertures.

[c2] A method according to claim 1, in which said hardmask layer is deposited by sputter deposition of Ta in an ambient containing N_2 and a carrier gas such that (N_2flow)/(N_2 + carrier flow) > 0.5.

[c3] A method according to claim 1, in which said hardmask layer is deposited by chemical vapor deposition by reacting a precursor gas containing Ta in an ambient containing N_2.

[c4] A method according to claim 2, in which said hardmask layer is substantially transparent in said relevant wavelength range.

[c5] A method according to claim 3, in which said hardmask layer is substantially transparent in said relevant wavelength range.

[c6] A method according to claim 2, in which said hardmask layer has a resistivity greater than about 400 μOhm-cm.

[c7] A method according to claim 3, in which said hardmask layer has a resistivity greater than about 400 μOhm-cm.

[c8] A method according to claim 2, in which said hardmask layer has a thickness ranging from 5nm to 100nm.

[c9] A method according to claim 3, in which said hardmask layer has a thickness ranging from 5nm to 100nm.

[c10] A method according to claim 2, in which said hardmask layer has a composition of less than 50% Ta.

[c11] A method according to claim 3, in which said hardmask layer has a composition of less than 50% Ta.

[c12] An integrated circuit comprising:
a semiconductor substrate containing a set of devices;
a first layer of interlayer dielectric (ILD) on a lower layer

of said integrated circuit above a set of lower alignment marks;

a first hardmask layer of TaN on said first layer of ILD, said first hardmask layer and said first ILD being substantially transparent in a relevant wavelength range;

an upper set of alignment marks;

a set of apertures in said ILD; and

a conductive interconnect in said set of apertures.

[c13] An integrated circuit according to claim 12, in which said hardmask layer is deposited by sputter deposition of Ta in an ambient containing N_2 and a carrier gas such that $(N_2 \text{flow})/(N_2 + \text{carrier flow}) > 0.5$.

[c14] An integrated circuit according to claim 12, in which said hardmask layer is deposited by chemical vapor deposition by reacting a precursor gas containing Ta in an ambient containing N_2.

[c15] An integrated circuit according to claim 13, in which said hardmask layer is substantially transparent in said relevant wavelength range.

[c16] An integrated circuit according to claim 14, in which said hardmask layer is substantially transparent in said relevant wavelength range.

[c17] An integrated circuit according to claim 13, in which said

hardmask layer has a resistivity greater than about 400 μOhm-cm.

[c18] An integrated circuit according to claim 14, in which said hardmask layer has a resistivity greater than about 400 μOhm-cm.

[c19] An integrated circuit according to claim 13, in which said hardmask layer has a thickness ranging from 5nm to 100nm.

[c20] An integrated circuit according to claim 14, in which said hardmask layer has a thickness ranging from 5nm to 100nm.

[c21] An integrated circuit according to claim 13, in which said hardmask layer has a composition of less than 50% Ta.

[c22] An integrated circuit according to claim 14, in which said hardmask layer has a composition of less than 50% Ta.